DESIGN AND SIMULATION OF INTEGRATOR USING THIN FILM TRANSISTOR BASED OPERATIONAL AMPLIFIER

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ABSTRACT

An Operational Amplifier is a basic building block of many analog and mixed signal systems. It is a high gain differential amplifier which can be used as summer, integrator, differentiator etc., and designed to operate at low voltage 3V DC. To design an Op-Amp, various electrical characteristics such as gain, bandwidth, slew rate, CMRR, output swing offset, etc., have to be taken in to account. Frequency compensation is necessary for closed loop stability since the op-amps are designed to be operated on negative feedback. An Integrator is an essential circuit component in many analog circuits that performs mathematical operation of Integration particularly in solving differential equation and can be used as a storage element in analog computing circuits. It is used where initial condition is of great importance and which affects the future calculations. The present research work proposes the basic use of integrator circuits in engineering design and simulation using Thin Film Transistor based Operational Amplifiers. This work also investigates the design of integrator circuit and the applications of the integrator. The designed circuits are very suitable for integrated circuit and implementation. The circuit performance is obtained through HSpice simulations and the results are compared with the existing theoretical work showing good agreement.

Keywords: Hspice, Integrator, Low Voltage, Operational Amplifier, Thin Film Transistor,.

I INTRODUCTION

Thin Film Transistor is popularly known as TFT, which are presently demanding more attention amongst the most common electronic devices. Since they introduced in the modern electronic industry and applications, TFTs have undergone extensive evolution, development and refinement. TFTs are three terminal devices, which belongs to IGFET family. TFT differs from a typical MOSFET in that it is composed of very thin layer deposited on an insulating substrate, whereas most MOSFETs are formed from a semiconductor wafer. TFTs are gaining more interest in large area electronics such as flexible displays, RFIDs, sensors, switching systems, solar cells, RAMs, low cost computer logic, flat panel for image crystallization etc,. They draw more attention towards the application of different types of TFTs, Mainly a-Si, and Poly-Si, increases need for an accurate and efficient material to simulate the circuits used on these devices.

Recently amorphous silicon TFT (a-Si TFT) and Poly Si TFT have become essential devices in many

applications especially in low cost ICs and large area integration. In this, a-Si TFT represent as mainstream technology for active matrix liquid crystal displays. Their advantages compared to crystalline MOSFETs are having low price and high capability of large area integration. These advantages compensates for low speed of a-Si TFT which is its main disadvantage. Although, Poly Si TFT have many more of the same applications as a-Si TFT its main advantages are both displays/switching and driver circuitry can be fabricated on the same chip and preferred in applications necessary for high speed. As their intended uses began from switching systems to low cost computer logic to flat panel display, addressing new materials, structures and fabrication techniques were introduced. A-Si TFT is the most widely used active layer material while Poly Si is increasingly pursued as a next generation TFT technology.

This paper is organized into the following sections. The detailed introductions about TFT is explained in Section I. The Section II, introduces the structures and modelling aspects of thin film transistor. Section III, dealt with the TFT Operational Amplifier circuit. Detailed design on TFT based Integrators and their analysis are discussed in section IV. Finally in section V, the result has been discussed and concluded in section VI.

1.1 Thin Film Transistors

Both in microelectronics and in low cost integrated circuits, Poly Silicon Thin Film Transistors (Poly-Si TFT) have become essential device due to its low temperature process. A leakage current (Ion, off current) present inconsistently in the device, is the problem of Poly Si TFT and this current is depend strongly on the bias and temperature which has been generated from grain boundary defects near the drain. It is very important to research on leakage current of Poly Si TFT and its reduction, because abnormal leakage current is the main deficiency of Poly Si TFT which is due to the field-assisted generation mechanism.

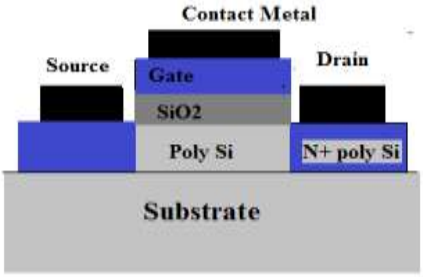

Fig. 1. Poly-Si Structure with Different Layers.

Fig.1 shows the structure of Poly Si TFT which is a kind of three terminal device; its substrate is floating just like SOI MOSFET. The modelling of Poly Si TFT is the effective medium of approach which treats the non-uniform poly silicon sample with grain boundaries as some uniform effective medium with effective material properties. The increase of drain current in saturation caused by the floating body effect. This short channel devices show a significant decrease of the sub-threshold idealistic factor with increasing drain voltage. By using the model, the relations of leakage current between terminal voltages, temperature of the TFT can be obtained.

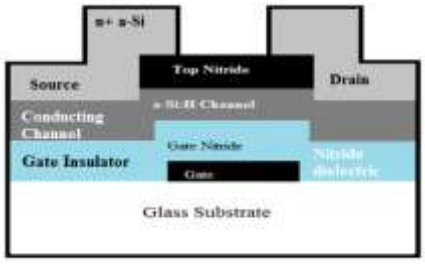

Fig. 2. Bottom Gate Structure of an a-Si:H TFT.

Fig.2 shows the bottom gate structure of a-Si:H TFT, also a three terminal device. The operation of a-Si TFT is quite different from that of crystalline MOSFETs. In the sub-threshold region the drain current is a poor function of the gate voltage dictated by large trap density in the material as in crystalline MOSFETs. Above the threshold, most of the induced charge in a-Si:H TFT are trapped and only a small fraction enters the conduction band. This fraction increases as the gate voltage increases. The field effect mobility increases with the gate voltage.

II OPERATIONAL AMPLIFIERS

2.1. Related Work

The CMOS OPAMP is widely used as analog building block for mixed signal circuits. Many OPAMP design is simple and robust, providing good values for its functional parameters. Palmisano, et al [1], explained about CMOS Op-Amp design procedure. This procedure has conditionally allowed using the compensation capacitor for limited range. In this design, Cc is the compensation capacitor greater than a parasitic capacitor C_{gs5} of TFT in the Op-Amp. The design procedure that allows the Cc a wider range and it would provide a higher degree of freedom in the trade-off between noise and power consumption which have been improved by Mahattanakul and Chutichatuporn[2]. A design procedure of multistage Op-Amp for settling time minimisation with low power is proposed by Pugliese, et al.[3]. When an Op-Amp is necessary to be operated at a high frequency, several limitations have come into the forefront in the existing approaches. The Op-Amp designed to work at a low voltage and low power has been improved by R. Kr. Baruah[4]. Although the simulation (Ehsan Kargaran, et al.)[5] done in HSPICE shows an operation at a low voltage and it consumes very low power, but an increase is observed in the UGF which is not noteworthy to be considered. The multi-stage designed proposed by Anshu Gupta, et al. 2010[6], leads to the decrease of the phase margin and UGF, but it improves the gain and settling time. It is very difficult that the transistors are in saturation condition when the supply voltage decreases (R. Gonzalez, et al.)[7]. In this research work an Op-Amp has been designed which exhibits high UGF for optimized balancing of gain, speed, power, phase margin, noise and load. Here, the proposed method is to set a higher UGF of the Op-Amp working at a low voltage supply. This permits the value of each circuit element of the amplifier i.e., transistor aspect ratios, bias current and compensation capacitor etc,. Frequency compensation is essential for two-stage and multi-stage Op-Amps and it has been analysed as done by Zushu Yan, et.al [8].

2.2. Ideal Operational Amplifier

An Op-Amp is the core component of surprisingly larger application in modern electronic era and undoubtedly one of the most useful mixed signal circuitry. The Op-Amp is usually, a single-ended output with a differential input of an electronic voltage amplifier of high gain. Its differential input is either NMOS input or PMOS input. Many operational amplifier systems are incorporating MOSFET transistors in design. This is true in low power and low voltage CMOS Op-Amp analog applications and act as functional core elements of mixed analog and digital Nano VLSI circuits and systems.

The main challenges of Op-Amp are a high dc gain and a high bandwidth with a high output swing depending on the applications. To achieve a higher gain, multi-stage Op-Amp can be used by cascading the stages [9]. If the gain is increased the bandwidth will be considerably reduced, which is the drawback of the two stage Op-Amp. However, it is difficult to compensate and hard to stabilize for the two- stage Op-Amp, which is widely used in many applications [10].

Frequency compensation technique is necessary to avoid closed loop instability. The easiest method for compensation is to connect a capacitor between input and output of the second stage [11]. This method gives high closed loop stability with lower bandwidth and results in splitting the poles. The Cascade compensation technique has been introduced to improve the stability in performance [12]. This technique improves the settling performance and the output swing is limited to certain range [13]. Single Miller Feed Forward Compensation technique is proposed and this technique improves stability and limits the bandwidth reduction [14]. However, this method suffers from compressed gain bandwidth problem because of very high gain of the first stage [15].

The circuit approach for the implementation of CMOS Op-Amp in the two stage configuration shown in Fig.3.

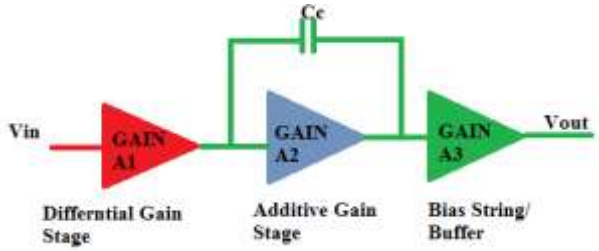

Fig. 3. Two Stage CMOS Op-amp.

It is designed to provide moderate gain and a relatively low UGF. The differential gain stage includes the input of the Op-Amp and provides the overall gain to improve off-set and noise performance. The additive gain stage improves its gain additionally and to allow maximum output swing. The final stage provides proper biasing and act as a buffer to convert impedance to low output impedance of additive gain stage and improves the current gain.

2.3. TFT Based Op-Amp

TFT have higher pinch-off voltage as compared with almost all the types of FETs. The TFT acts as a switching device in most of the applications. The switching is closed in microseconds and opened it in milliseconds. Like CMOS device characteristics, TFTs are having high immunity to noise, operates on low power voltage and low static power consumption.

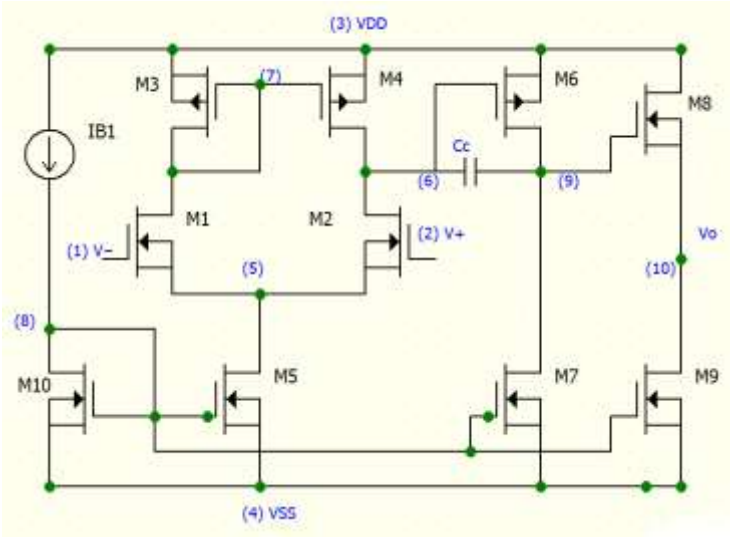

Fig. 4. Two Stage Hybrid Op-Amp with n-channel Input Stage

As MOSFET, significant power is drawn only when TFT device is switching between on and off states and it is not producing much heat as other forms of logic. These devices also allow a high density of logic functions on a chip. TFTs operate on low power voltage and low static power consumption like MOSFET and CMOS, but they are highly immunity to noise. When TFT device is switching between on and off states, it draws less power. Also, they are not producing much heat as MOSFETs. These TFT devices also allow a high density of logic functions on a chip.

In our previous work [16-21], we designed an Op-Amp using a-Si TFT and Poly-Si TFT. Also, we discussed about the design constraints which leads to a well-designed Op-Amp and explained the reason for using two types of TFT devices such as amorphous Si TFT and Poly-Si TFT. Our proposed design of a two stage TFT based Op-Amp circuit is shown in Fig.4. Simulations are carried out on the design of both the TFTs as well as CMOS based Op-Amps. In TFT based Op-Amp, TFTs are used as n-type MOSFET while p-type MOSFET are used as complementary devices.

2.4. Detailed Designed Procedure

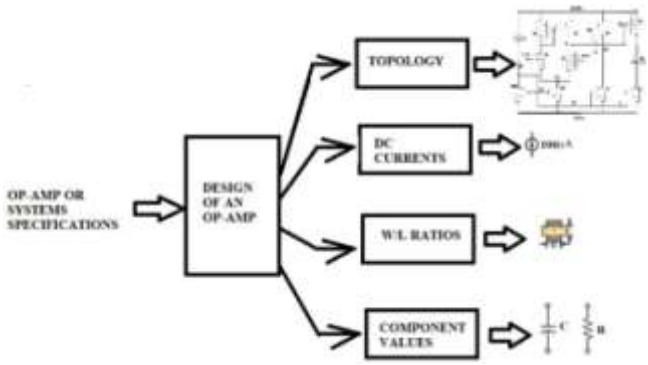

Fig.5.Design Procedure of an Op-Amp

The design procedure of proposed Op-amp is described in Fig.5, with required basic fundamental data shown in Table.1 for procedural technique to design an Op-amp. The design procedure carried out for the Op-amp using both TFTs and CMOS. The design specification used for calculation is shown in Table.1. The designed

Op-Amps have been simulated using HSpice Circuit Simulator and the final design specifications have been shown in Table.2. The performances of Op-Amps are shown in Table.3 obtained from the recorded values.

III INTEGRATOR USING TFT OP-AMP

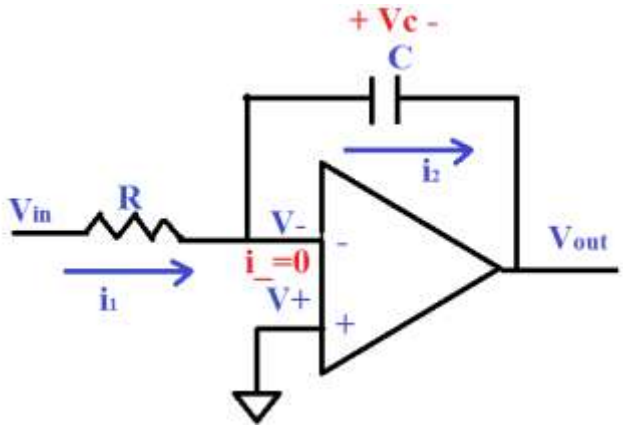

Fig.6.Ideal Inverting Integrator Circuits using an Op-Amp

The Integrator is a circuit using OP-AMP which performs the mathematical operation of Integration. The integrator acts like a storage element with respect to time, that produces an output voltage which is directly proportional to the integral of voltage applied in the input. In other words, the magnitude of the signal output is calculated by the duration of time an input voltage is present as the current flows through the capacitor which is required for negative feedback. The circuit shown in Fig.6 is an ideal inverting integrator, since the input is applied to the inverting input of the Op-Amp. Mixed Mode signal is used for the simulation of the integrator. Since the circuit uses the inverting configuration, we conclude that the circuit transfer function is:

$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{Z_2(s)}{Z_1(s)} = -\frac{1/sC}{R} = \frac{-1}{sRC} \quad -----(1)$$

In other words, the output signal is related to the input as:

$$V_{out}(s) = \frac{-1}{RC}\frac{V_{in}(s)}{s} \quad ----------(2)$$

It means that the output signal is proportional to the integral of the input signal. We can prove that the circuit integrates the input by taking the inverse Laplace Transform:

$$V_{out}(s) = \frac{-1}{RC}\int_0^t \frac{V_{in}(t')}{s}dt' \quad ----------(3)$$

If the input is: $V_{in}(t) = \sin \omega t \quad ----------(4)$

Then the output becomes $V_{out}(t) = \frac{-1}{RC}\int_0^t \sin \omega t dt' = \frac{-1}{RC}\frac{-1}{\omega}\cos \omega t = \frac{1}{\omega RC}\cos \omega t \quad --(5)$

The same result may be obtained using Fourier analysis also:

$$G(\omega) = \frac{V_{out}(\omega)}{V_{in}(\omega)} = \frac{Z_2(\omega)}{Z_1(\omega)} = -\frac{1/j\omega C}{R} = \frac{j}{\omega RC} \quad -----(6)$$

Thus, the magnitude of the transfer function is:

$$|G(\omega)| = \left|\frac{j}{\omega RC}\right| = \frac{1}{\omega RC} \quad ----------(7)$$

And since: $j = e^{j(\pi/2)} = \cos(\pi/2) = j\sin(\pi/2)$ ----------(8)

The phase of the transfer function is:

$$\angle G(\omega) = \pi/2 \, radians \quad = 90° \quad ----------(9)$$

Also also the same result may be determined using time domain analysis. From the Fig.6, the voltage across the capacitor is: $V_c(t) = \frac{1}{C}\int_0^t i_2(t')dt'$ ----------(10)

And from the circuit: $V_c(t) = V(t) - V_{out}(t) = -V_{out}(t)$ ----------(11)

Therefore, the output voltage is: $V_{out}(t) = \frac{1}{C}\int_0^t i_2(t')dt'$ ----------(12)

There by it is proved that by using any one of the method we can determine the same result. The practical Integrator is shown in Fig.7. When $V_{in} = 0$, the integrator gives open loop gain because capacitor acts as a open circuit for DC voltage, which means that the input offset voltage of the Op-Amp which produces voltage at the output is an error. Therefore to acquire output voltage without error, a resistor is connected in parallel with the feedback capacitor. The various applications of Op-Amp Integrator are available in the industry. In this paper, we described the Ramp Generator and analyzed its performance.

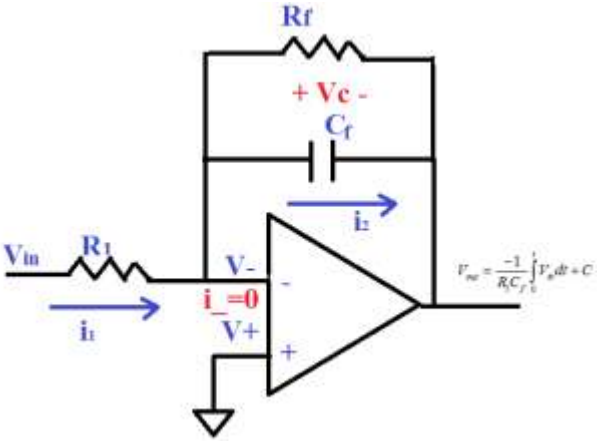

Fig.7.Practical Inverting Integrator Circuits using an Op-Amp

3.1. Ramp Generator

The integrator integrates the current I across capacitor C_1 when the same current I is flowing through resistor R_1. The voltage across C_1 is called as output voltage V_{out}. One of the great application of the integrator is that the ramp voltage is generated by it. This can be generated by placing a fixed voltage at V_S that develops a constant current through R_1. The capacitor then integrates this current and generates a ramp voltage. The circuit essentially integrates the input current $I_s = V_s / R_1$ across capacitor C_1. The output

voltage is realized as capacitor voltage after a time interval T, described by: $V_{out} = \frac{-1}{C_1}\int_0^T \frac{V_S}{R_1}dt$. When a constant input voltage is applied at V_S, the output ramp voltage increases steadily. The output voltage (ramp) at any time T can be predicted by the simplified equation: $V_{out} = \frac{-1}{C_1} x \frac{V_S}{R_1} xT$

The response of generating ramps can be increased or decreased than the original circuit by changing the value of V_S, R_1 or C_1. From the principles of integration, it describes that voltage across the capacitor is equal to ratio of the charge on the capacitor to its capacitance, ie., Q/C. Then the voltage across the capacitor is output V_{out} therefore: $-V_{out} = Q/C$. The rate of change of voltage across the capacitor due to charging and discharging of the capacitor, is given as:

$$V_C = \frac{Q}{C}, \qquad V_C = V_X + V_{out} = 0 + V_{out}, \quad -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C} x \frac{dQ}{dt} \text{ ---------- (13)}$$

Where dQ/dt is an electric current. Since inverting input terminal of integrating Op-Amp is zero, X = 0, the input current I_{in} is flowing through the input resistor R_{in} is given by the equation:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}} \text{ ---------- (14)}$$

The current flowing through the capacitor C is given by the equation:

$$I_{in} = C\frac{dV_{out}}{dt} = Cx\frac{dQ}{Cdt} = \frac{dQ}{dt} = C\frac{dV_{out}}{dt} \text{ ---- (15)}$$

Assuming that input impedance of the Op-Amp is infinite as an ideal Op-Amp, no current flows into the Op-Amp terminal. Therefore, the nodal equation at the inverting input terminal is given by the equation:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = C\frac{dV_{out}}{dt}, \quad \therefore \frac{V_{in}}{dV_{out}}\frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the Op-Amp used in the Integrator as:

$$V_{out} = \frac{-1}{R_{in}C}\int_0^t V_{in}(t)dt \text{ ---------- (16)}$$

This equation can also be re-written as:

$$V_{out} = \frac{-1}{j\omega RC} xV_{in} \text{ ---------- (17) Where } j\omega = 2\pi f$$

and the output voltage V_{out} is a constant 1/RC times the integral of the input voltage V_{in} with respect to time. The minus sign (-) indicates a 180°phase shift, because the input signal is connected directly to the inverting input terminal of the op-amp. In this paper, we investigate the performances of ramp generator by using TFT based Op-Amp and the circuit is simulated in HSpice Circuit Simulator and the output is shown in Fig.7a, Fig.7b and Fig.7c.

IV RESULTS AND DISCUSSIONS

Table-1: Design Parameters

DESIGN AND SPICE PARAMETERS			
Parameter	**Poly Si TFT**	**a-Si TFT**	**CMOS**
V_{DD}	+3V	+3V	+3V
V_{SS}	-3V	-3V	-3V
Ao	≥1000	≥1000	≥15000
GB= 2π(X)	1.5MHz	20KHz	5MHz
SR (V/µS)	5	2.2	10V/µS
PM	>80°	>85°	>60°
Ro	≤3.5K	≤1.5K	≤1.46K
λ	0.04	0.04	0.02
V_{eff}	2.25V	1.8V	2.25V
$K_n(\mu A/V^2)$	2.62	1.35	40
$K_p(\mu A/V^2)$	48.74	48.74	15
CMR	-2.5 ≤ , ≤ 1.2	-2.65 ≤ , ≤ 0.65	-2.5 ≤, ≤ 1.75
C_C	1pF	1pF	1pF

The design and Spice parameters used for calculation of various parameters of the proposed design of Op-Amp using Poly Si TFT, a-Si TFT and CMOS is shown in Table 1. After the calculation, values are obtained to be used in simulation which is shown in Table-2, for all the three Op-Amps. From the Table-2, we observed that the size of the Poly Si TFT Op-Amp is 0.57% smaller than CMOS Op-Amp. Also the current consumed in the CMOS Op-Amp is 3.37µA more than Poly Si TFT Op-Amp. Using HSpice circuit simulator, the result has been summarized in the Table -3 for comparison of both the Operational Amplifiers. From the Table-3, the Gain A_{VO} of CMOS Op-Amp is more than 10 times of Poly Si TFT Op-Amp and Slew rate and Unity gain bandwidth are almost 3 times better than Poly Si TFT Op-Amp. But the Phase Margin is almost near to 90° in Poly Si TFT Op-Amp and considerably less in CMOS Op-Amp. Output Resistance is double in Poly Si TFT Op-Amp than CMOS Op-Amp. CMRR of Poly Si TFT Op-Amp is considerably less than CMOS Op-Amp. These Op-Amps are used in the proposed Integrator design and specifications are shown in Table-4. The performances of all the three integrators in the form of graph after simulation are shown in Fig.7a, Fig.7b, and Fig.7c. The output of a-Si TFT is slightly degraded from the output of Poly Si TFT and CMOS based Integrators.

Table -2: TFT Based Op-Amp Design Specification

(L=6.6µm and Leff=5.6µm are used)

PAR	Poly Si TFT Op-Amp			a-Si TFT Op-Amp			CMOS Op-Amp		
	I (µA)	**W/L**	**W (µm)**	**I (µA)**	**W/L**	**W (µm)**	**I (µA)**	**W/L**	**W (µm)**
M1	3.315	6.33	35.5	0.962	18.85	105.9	5	6.53	36.6
M2	3.315	6.33	35.5	0.962	18.85	105.9	5	6.53	36.6
M3	3.315	0.625	3.5	0.962	1.11	6.2	5	0.96	5.4
M4	3.315	0.625	3.5	0.962	1.11	6.2	5	0.96	5.4

M5	6.63	5.36	30.0	1.924	37.5	210.0	10	5.36	30
M6	30	6.32	35.4	12.03	14.5	81.2	30	5.79	32.4
M7	30	14.8	83.0	12.03	21.2	118.8	30	16.07	90
M8	100	156	873.6	75.33	2742.7	15359.1	100	156	873.6
M9	100	53.57	300	75.33	166.6	933.0	100	53.33	300
M10	100	53.57	300	100	166.6	933.0	100	53.33	300

TABLE- 3: Op-Amp Performance

Parameters	**Simulation Results**		
	Poly Si TFT	**a-Si TFT**	**CMOS**
Gain	1.2496K	15.1003K	16.7618K
UGB	1.35 MHz	120.17 KHz	5.45 MHz
CMRR	253.638	1.3317K	34.182K
Slew Rate (V/µS)	6.92	3.94	7.93
Dc Offset Voltage (µV)	740.7155	-688.75	197.62
Power Dissipation (m.Watts)	1.4354	1.1357	1.4690
Output Resistance (KΩ)	3.7118	10.1345	1.3919
Phase Margin	80°	83.16°	54°
Open loop Gain Margin (dB)	84.5	83.6	84.5

TABLE- 4: Integrator Specification

Parameters	**Integrator Using**		
	Poly Si TFT	**a-Si TFT**	**CMOS**
V_{DD} (V)	3	3	3
V_{SS} (V)	-3	-3	-3
Resistance R_1 (Ω)	50K	450K	50K
Resistance R_2 (Ω)	1MEG	1MEG	1MEG
Capacitor C_f (µF)	0.017	0.001	0.010
Resistance R_L (Ω)	50K	50K	50K
DC Voltage Gain (dB)	20	2.22	20

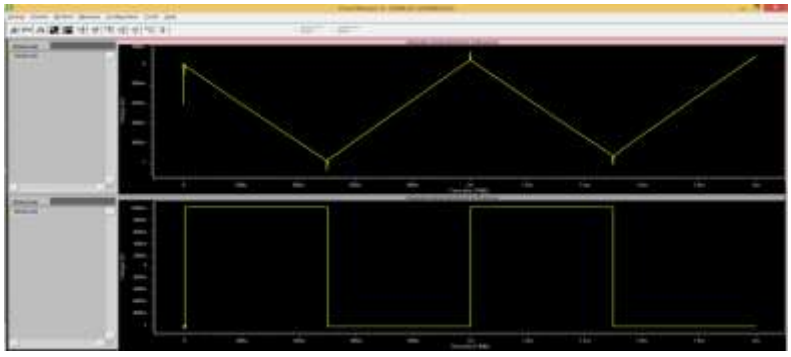

Fig.8a. Input and Output of Poly Si TFT Op-Amp.

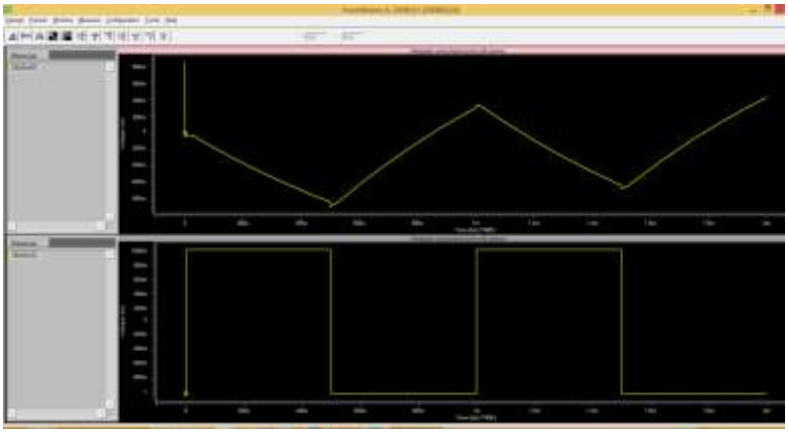

Fig.8b. Input and Output of a-Si TFT Op-Amp.

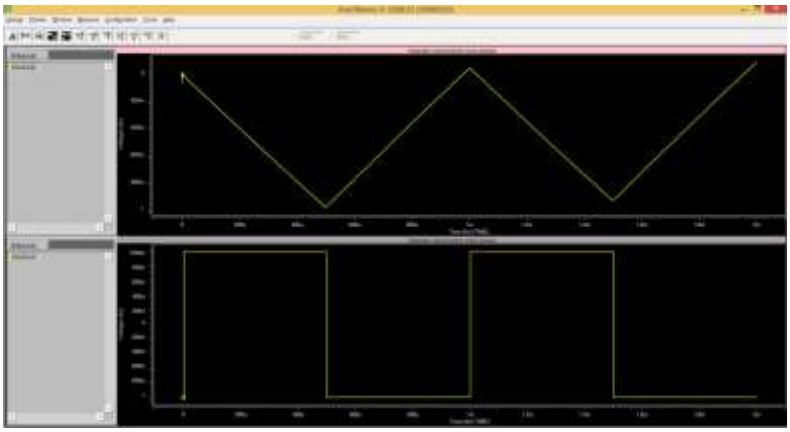

Fig.8c. Input and Output of CMOS Op-Amp.

V CONCLUSION

Poly Si TFT based Op-Amp is performing well as compared to CMOS Op-Amp. Though Gain, Slew rate, and frequency of operation of CMOS Op-Amp is better performing than Poly Si TFT Op-Amp, but Poly Si TFT Op-Amp have better stability and robustness to failure, because of high phase margin and double the output resistance. The TFT and CMOS Op-Amp, used for the Integrators design are generating the Ramp signal output which agrees with the existing theoretical and practical work. But the a-Si TFT based Integrators slightly degraded than Poly Si TFT and CMOS based Integrators which are suitably agreed with the theoretical and existing research works [22]. When $v_{in} = 0$, the integrator gives open loop gain because capacitor acts as an open circuit for DC voltage. Input offset voltage of the Op-Amp which produces an error voltage at the output. To obtain error free output voltage resistor $R_2$is connected in parallel with the feedback capacitor. The error is almost reduced in all the three Integrators output. But the CMOS Integrators are produced excellent output with least error output voltage compared to TFT based Integrators. DC output gain of Poly Si TFT and CMOS based Integrators are 10 times more than a-Si TFT based Integrators. This paper concludes that the characteristics of Op-Amp limits the performance of the Integrators as the characteristics of the transistors used in the Op-Amp decides its performance. All the three Op-Amps are suitable for any applications as seen from the results.

REFERENCES

[1] Palmisano, G., Palumbo, G., and S. Pennisi, (2001). *Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial.* Analog Integrated Circuits and Signal Processing, *Volume 27, Issue 3, pp 179-189,* May 2001. DOI 10.1023/A: 1011229119071. ISSN: 0925-1030

[2] Mahattanakul, J. and Chutichatuporn, J., (2005). *Design Procedure for Two- Stage CMOS OPAMP with Flexible Noise-Power Balancing Scheme.* IEEE Transaction on Circuits and Systems-I: Regular Paper *vol. 52, no. 8, pp. 1508-1514.* DOI: 10.1109/TCSI.2005.851395.

[3] Pugliese, A , Cappuccino, G. and Cocorullo, G., (2008). *Design Procedure for Settling Time Minimization in Three-Stage Nested Miller Amplifiers.* IEEE Transaction on Circuits and Systems-II *Volume 55, Issue 1, pp. 1-5,* Jan 2008. DOI: 10.1109/TCSII.2007.906086.

[4] Baruah, R. Kr., (2010). *Design of A Low Power Low Voltage CMOS Opamp*. International Journal of VLSI Design & Communication Systems, *Volume 1, Number 1,* March 2010. DOI: 10.5121/vlsic.2010.1101.

[5] Ehsan Kargaran, Hojat Khosrowjerdi and Karim Ghaffarzadegan, (2010). *A 1.5 V High Swing Ultra- Low-Power Two Stage CMOS OP-AMP in 0.18 µm Technology.* 2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010). IEEE Catalog Number: CFP1016K-PRT, ISBN: 978-1-4244-7479-0. Published in International Journal of Science and Research (IJSR), India, *Volume 2 Issue 3,* March 2013. DOI:10.1109/ICMEE.2010.5558594.

[6] Anshu Gupta and D.K. Mishra, R. Khatri, (2010). *A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology.* Computer Information Systems and Industrial Management Applications (CISIM), 2010 on 08-10,Oct 2010, pp. 448 – 453, Nov.2010. DOI: 10.1109/CISIM.2010.5643497.

[7] Gonzalez, R.., B.M. Gordon, M.A Horowitz, (1997). *Supply and Threshold voltage scaling for low power CMOS.* IEEE journal of solid state Electronics, *Vol 32, No 8,* August, 1997, DOI: S 0018-9200(97)05302-X.

[8] Zushu Yan, Pui-In Mak, and Rui P. Martins, (2011). *Two-Stage Operational Amplifiers: Power-and-Area-Efficient Frequency Compensation for Driving a Wide Range of Capacitive Load.* IEEE Circuits and Systems Magazine,1531-636X/11/$26.00©2011, DOI: 10.1109/MCAS.2010.939783.

[9] Ramirez-Angulo, J (2007). *Low-voltage, low-power rail-to-rail two stage op-amp with dynamic biasing and no Miller compensation.* In the Proceeding of the 50th Midwest Symposium on Circuits and Systems, MWSCAS, pp:25-28, Aug. 5-8, 2007, Quebec, Canada. ISBN: 978-1-4244-1175-7, DOI:10.1109/MWSCAS.2007.448853.

[10] Rosario,M., P.Gaetano and P.Salvatore (2003). *Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers.* IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, 50(5): 227-233, 2003. DOI: 10.1109/TCSII.2003.811437.

[11] Amana,Y (2012). A Review Paper on Design and Synthesis of Two-Stage CMOS Op-Amp, International Journal of Advances in Engineering and Technology, 2(1): 677–688, 2012, ISSN: 2231-1963.

[12] Singh,R. and G.Anu (2011). *Design on Fully Differential Op-amp for High Stability.* In the Proceedings of the International Conference on Electric and Electronic, pp: 1–5, Coimbatore, India, 2011.

[13] Vaibhav,K. and C.Degang (2009). *Design Procedure and Performance Potential for Operational Amplifier using Indirect Compensation.* In the Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems, pp: 13-16, Aug. 2-5, 2009, Cancun, Mexico. ISBN:78-1-4244-4479-3 DOI:10.1109/MWSCAS.2009.5236165

[14] Pugliese,A., F.A.Amoroso, G.Cappuccino and G.Cocorullo (2008). *Settling-time-oriented design procedure for two-stage amplifiers with current-buffer Miller compensation.* In the Proceeding of the 4th European Conference on Circuits and Systems for Communications, pp: 114-117, Jul. 10-11, 2008, Bucharest, Romania. DOI:10.1109/ECCSC.2008.4611658

[15] Gupta,A (2010). *A two stage and three stages CMOS OPAMP with fast settling, high DC gain and low power designed in 180nm technology.* In the Proceedings of the International Conference on Computer Information Systems and Industrial Management Applications (CISIM), pp: 448-453, Oct. 8-10,2010, Venice, Italy. DOI:10.1109/CISIM.2010.5643497.

[16] Prabhakaran,G., and V.Kannan (2011). *Analysis and Modelling of Hybrid Operational Amplifiers Using Amorphous Silicon Thin Film Transistor.* CiiT International Journal of Programmable Devices Circuits and Systems, Vol 3, No 12, September 2011, DOI: PDCS092011007.

[17] Prabhakaran,G., and V.Kannan (2013). *Design and Analysis of Hybrid Operational Amplifiers Using Poly-Si Thin Film Transistor for Low Voltage Applications.* Proceedings of International Conference on Global Innovations in Technology and Sciences -4th to 6th April, 2013. Published in International Journal of Scientific & Engineering Research (IJSER), Volume 4, Issue 8, August 2013, ISSN 2229-5518.

[18] Prabhakaran,G., and V.Kannan (2014). *Low Voltage Application of Hybrid Op-Amp Using Thin Film Transistor In Summing Amplifier.* Published in Vol. 29 (no 7, Year 2014) of Ciencia e Tecnica Vitivinicola journal (ISSN:0254-0223). URL:http://ciencia-e-tecnica.org/cien/index.php/archive/part/29/7/1/?CurrentVol =29 &currentissue=7.

[19] Prabhakaran, G., and V.Kannan(2014). *Design Configuration of Circuit and Comparison of Hybrid TFT Op-Amp with its CMOS Counterpart.* Presented in Second National Conference On Advancements And Future Trends in VLSI Design (NCVD'14) in Kalasalingam University on 26 Sep 2014, Proceedings pp-1-9. And Published in International Journal of Digital Communication and Networks (IJDCN), *Vol 1, Issue 3,* September 2014, ISSN: 2345-9850. URL: http://ijdcn.co.in/issuecategory/volume-3-september-2014.

[20] Prabhakaran, G., and V.Kannan (2015). *Design and Analysis of Thin film Transistor Based Operational Amplifier.* Published in *Vol. 159, Issue. 1* of Sylwan journal (ISSN: 0039-7660), Jan 2015.

[21] Prabhakaran, G., and V.Kannan (2015). *Comparative Analysis of Thin film Transistor Based Operational Amplifier.* Presented in Second International Conference on Green Technologies for Power Generation, Communication & Instrumentation (ICGPC'15) on 26th and 27th Jan 2015, St. Peter's University, Chennai.

[22] Pratibhadevi Tapashetti, Ankur Gupta, Chandrashekhar Mithlesh, A.S Umesh, (2012). *Design and Simulation of Op Amp Integrator and Its Applications.* International Journal of Engineering and Advanced Technology (IJEAT), *Volume-1, Issue-3*, pp 12-19, February 2012, ISSN: 2249 – 8958.

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