# A SURVEY ON ANALYSIS OF LOW POWER AND LOW VOLTAGE OF COMPARATORS

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## ABSTRACT

*Design of low voltage double-tail Comparator with pre-amplifier and latching stage is reported in this paper. Design has specially concentrated on delay of both single tail comparator and double-tail comparator, which are called clocked regenerative comparator. Based on a new dynamic comparator is proposed, where the circuit of conventional double tail dynamic comparator is modified for low power and fast operation even in small supply voltages. Simulation results in 0.25µm CMOS technology confirm the*
*analysis results. It is shown that proposed dynamic comparator both power consumption and delay time reduced. Both delay and power consumption can be reduced by adding two NMOS switches in the series manner to the existing comparator. The supply voltages of 1.5V while consuming 1 5µw in proposed comparator and 16 µw in existing comparator respectively.*

***Keywords: Double Tail Comparator, Low-Power Analog Design, Power Gating Technique, Tanner EDA Tool.***

## I. INTRODUCTION

Comparator is one of the fundamental building blocks in Analog-to-digital converters. designing high speed comparator is more challenging when the supply voltage is smaller. in other words to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Developing a new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low voltage operation, especially if they do not increase circuit complexity.
Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low voltage operation.
Many high speed ADC's such as flash ADC's requires high speed, low power comparators with small chip area. A new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

## II. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decision due to the strong positive feedback in the regenerative latch. Recently many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset and random decision errors and kickback noise

### 2.1 Conventional Dynamic Comparator

This comparator widely used in A/D converters with high input impedance, rail-to-rail output swing and no static power consumption. Fig 1 shows the Schematic diagram of the conventional Dynamic comparator.

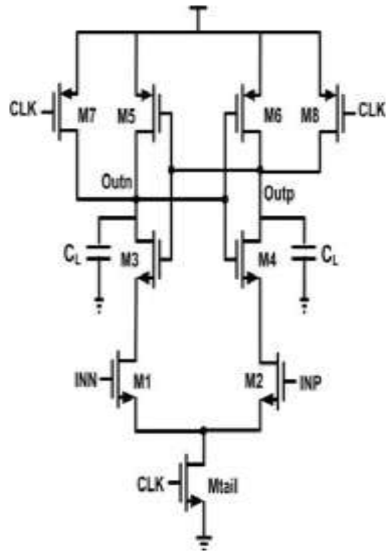


**Fig. 1 Schematic diagram of a conventional Dynamic Comparator**

The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off ,reset transistors (M7– M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. After when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre- charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor *M*2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor *M*1 drain current), the corresponding PMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa. The simulation of the comparator is shown in Fig 2.

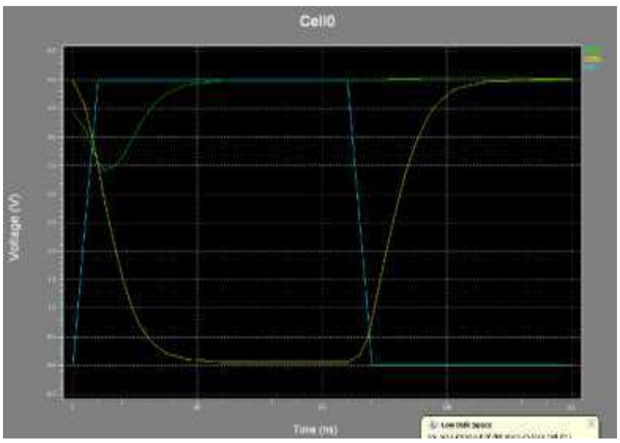


**Fig.2. Transient simulation of the conventional dynamic comparator**

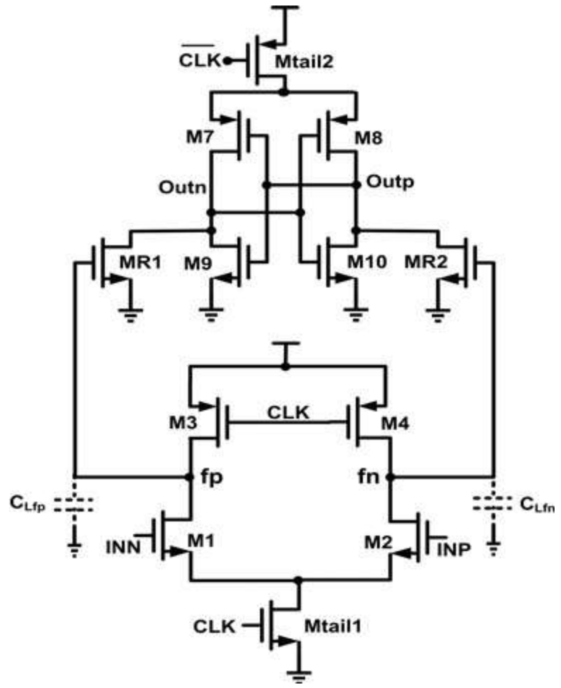


**Fig.3 Schematic diagram of the conventional double-tail dynamic comparator.**

### 2.2 Conventional Double Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig .3. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset. During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground.

During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by I Mtail1/Cfn(p) and on top of this, an input dependent differential voltage ΔVfn(p) will build up. The intermediate stage formed by MR1 and MR2

passes ΔVfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. Fig 4 shows the simulation of this comparator.

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus t0 is obtained where IB1 is the drain current of the M9 and approximately equal to the half of the tail current.

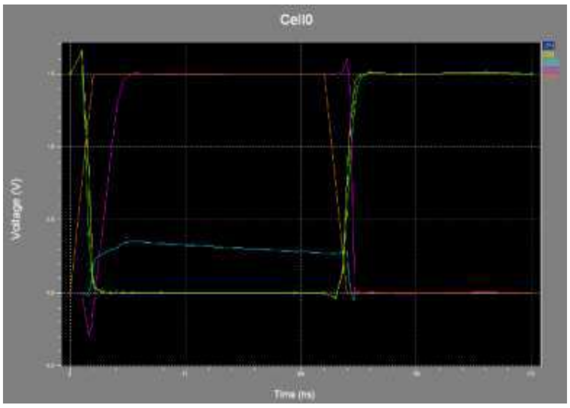


**Fig.4. Transient simulation of the conventional double tail dynamic comparator**

## III. PROPOSED DOUBLE TAIL DYNAMIC COMPARATOR

Fig 5 Shows the Schematic diagram of the proposed method. The operation of the proposed comparator is as follows. During reset phase (Clk=0 Mtail1 and Mtail2 are off avoiding static power),M3 and M4 pulls both fn and fp nodes to VDD hence Mc1 and Mc2 are cut off .Intermediate stage transistor MR1 and MR2 reset both latch outputs to ground.

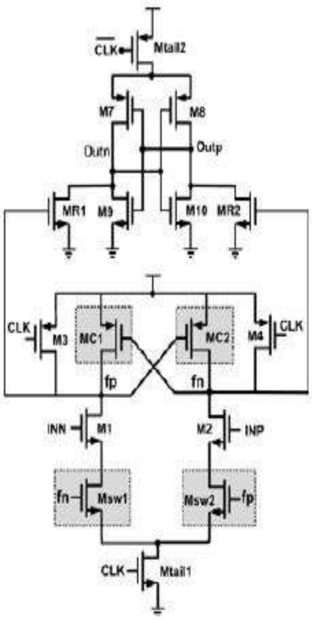


**Fig.5.Schematic diagram of proposed double-tail dynamic comparator**

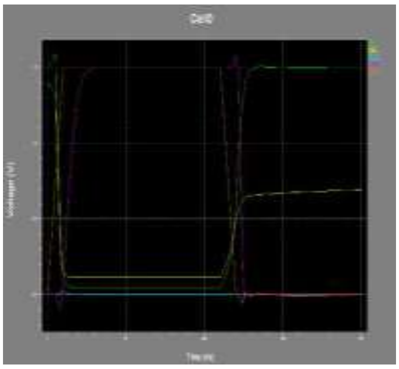

**Fig.6 Transient simulation of the proposed double-tail dynamic comparator**

During decision making phase (CLK=VDD Mtail1,and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP>VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding PMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a PMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g.,Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, andMtail1) as shown in Fig 6, resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistor.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been precharged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. Future work is the delay of the proposed double tail dynamic comparator to be reduced from the present delay value.

## IV. PERFORMANCE COMPARISON

**TABLE 1**

| **Comparator Structure** | **Single Tail Comparator** | **Conventional Double Tail Comparator** | **Proposed Double Tail Comparator** | **Modified Double Tail Comparator** |
|---|---|---|---|---|
| Technology CMOS | 180 nm | 180 nm | 180 nm | 180 nm |
| Supply voltage (v) | 0.8v | 0.8v | 0.8v | 0.8v |
| Power Consumption (watts) | 7.04 x 10-6 watts | 1.50 x 10-5 watts | 1.29 x 10-5 watts | 9.50 x 10-6 watts |
| Delay (sec) | 6.61 x 10-8 sec | 7.51 x 10-9 sec | 7.48 x 10-9 sec | 4.84 x 10-9 sec |

## V. SIMULATION RESULTS

In order to compare the proposed comparator with the single tail comparator and the conventional double tail comparators, all circuits have been simulated in 180 nm CMOS technology, VDD = 0.8v. Tanner EDA Tool is a leading provider of easy to use, PC based electronic based design automation (EDA) software solution for the design, layout and verification of analog – mixed signal integrated circuits. The result is simulated in T-SPICE platform and the circuit has been drawn using S-EDIT and got the output waveform in W-EDIT. Using the Tanner EDA Tool each comparator circuits has been simulated and got the output waveforms, which show the corrective working of the designed circuits. T-SPICE gives the power consumption and delay analysis results. For the simulation of all comparator structures, the supply voltage (VDD) given is 0.8v, the input voltage INP given is 0.7v and INN given is 0.5v. For each circuit structures the number of transistors used varies. The simulation results show that for the proposed double tail comparator, the power consumption is reduced drastically when comparing all other comparator structures.

## VI. CONCLUSION

The paper, presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-µm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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