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MONTE-CARLO SIMULATION FOR 9T SRAM CELL IN 45NM CMOS

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ABSTRACT

Due to seriousness of process variation in deep sub-micron devices, it is necessary to study the operation of the ratioed structure under process variations and device mismatch. The global and local variations can cause the traditional ratioed logic to lose functionality. The Static Random Access Memory (SRAM) is highly ratioed and affected by the global and local process fluctuations. In this paper, the proposed SRAM cell has been investigated for the statistical process variations. The cell shows the improved read stability and write ability due to isolation of read and write circuits. The cell shows robustness against temperature, process and voltage variation due to separate write signal WS, lower leakage current and lower parasitic capacitance.

Key Words: SRAM cell, Local and global variations, Monte Carlo Simulation, Leakage current, Power consumption

I. INTRODUCTION

SRAM is a critical component in memory rich System on Chip (SoC) design. The conventional 6T SRAM cell has large storage capacity but still suffers from large dynamic power consumption, large leakage current and degraded read stability. Various sub threshold SRAM cells [1-5] have been proposed to reduce the power consumption of the cell. Researchers have also proposed the new design technique to improve the stability of the cell as well as to reduce the overall power consumption [6-10]. Since now a day's SRAM cell is designed in the deep sub-micron region, hence the extreme global and local variations and device mismatch causes the cell to lose its functionality. Due to increased threshold voltage fluctuations caused by global and process variations, SRAMs suffer from instability in write and read operations.

In this paper, we have studied the statistical variation in terms of process, voltage and temperature (PVT) for the proposed cell. The cell has distinct read and write port to improve read stability. The write operation is performed with separate signal instead of conventional WL. The robustness of the cell is established against the process variation after performing the Monte Carlo Simulation. The rest of the paper is organized as follows; section II deals with architecture and simulation results whereas section III concludes the paper.

II. ARCHITECTURE OF CELL

The architecture of the power efficient 9T SRAM cell is shown in Figure 1. The discharging activity of the cell on bit line is reduced during write operation due to write signal WS. The leakage current also restricted in the cell during write and read operations. The uses of separate write signal WS improves the write margin of the cell. The cell has distinct ports for write and read operations which enhance the read stability. Depending upon the write

operation, signal WS is chosen as; WS=0 for write 1 and WS=V_{dd} for write 0. When WS=0, transistor NM0 turns off and hence node Q flips to high without waiting BL has to discharge. This is write 1 operation. For write 0 operation, connect WS to Vdd which makes transistor PM0 off and hence logic 0 will result at node Q.

During read operation, depending upon the data on the storage node QL, the precharged RBL either discharges through three series connected ON transistors or maintains its voltage level.

Due to single read and write bit line/wordline, parasitic capacitance of the cell is reduced which further lowers the power consumption in the cell.

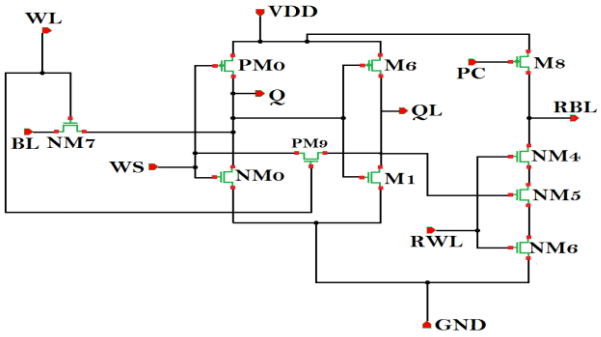

Figure 1: Architecture of the 9T cell.

III. SIMULATION RESULTS AND DISCUSSION

The proposed cell is simulated in terms of statistical PVT (process, voltage, temperature) variation at V_{dd}=0.8V using HSPICE 45nm model parameters at the layout level. The lower voltage drop on the BL, due to signal WS, (Figure 2) results in lower dynamic power during write operation. Due to two series connected OFF transistors in the read circuit, the leakage current reduces drastically. The reduced dynamic power and lower leakage current results in lower write power consumption. Figure 3 shows the robustness of the 9T power efficient cell against temperature. The write 0 operation remains unaffected with the temperature whereas a small disturbance in the write 1 operation is observed as the temperature rises above 40^0C.

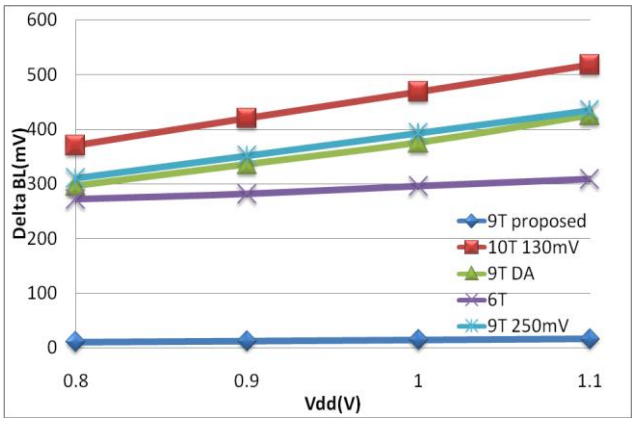

Figure 2: Voltage Drop on Bitline During Write Operation

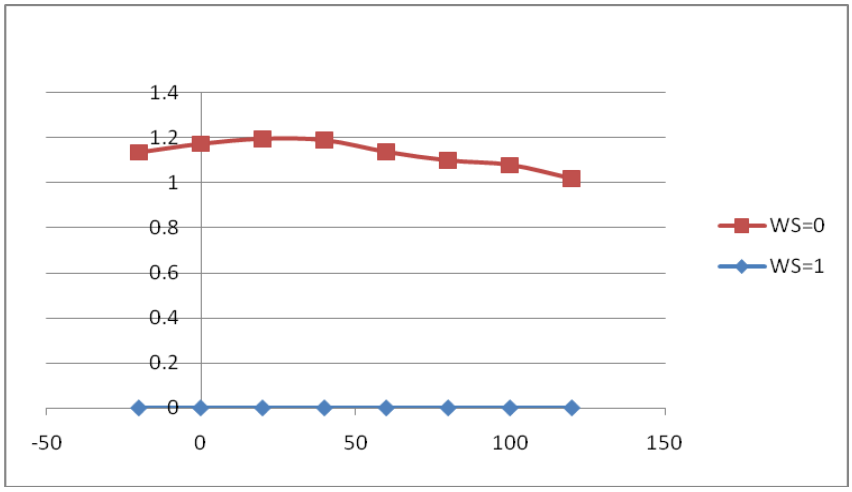

Figure 3: Varaiation of Node Voltage with Temperature

In order to evaluate the effectiveness of the proposed cell against process variation, we have performed the Monte Carlo (MC) simulation for write ability, read operation and hold mode. Figure 4 shows the MC simulation for the threshold voltage. The nominal threshold voltage of the transistor is 500mV. The simulation was performed for N=2500. The result shows a larger value of the mean and lower value of standard variation. The larger mean value reflects the robustness of the threshold voltage of the transistors in the cell against any random variation.

The MC simulation has been performed for the ΔBL for N=1000 as shown in Figure 5. It is observed that mean voltage drop on bit line is very small in the proposed cell compared to the other cells. The proposed cell also gives lower standard deviation.

The MC simulation was carried out for the hold SNM (static noise margin) for N=1000 and TT process corners at T=27^{0}C. From simulation results (Figure 6(a)) it is observed that the proposed cell gives 1.1x higher mean hold SNM compared to the 250mV Cell [6] and 1.03 xs compared to the DA cell [8]. Further, standard deviation is reduced approximately 26% compared to the 250mV cell [6]. Figure 6(b) shows the MC simulation for hold 1 power consumption (N=1000 at V_{dd}=0.8V and T=27^{0}C). The simulation results show lower mean power consumption and lower standard deviation. This is due to restricted leakage current in the read/write circuits of the cell.

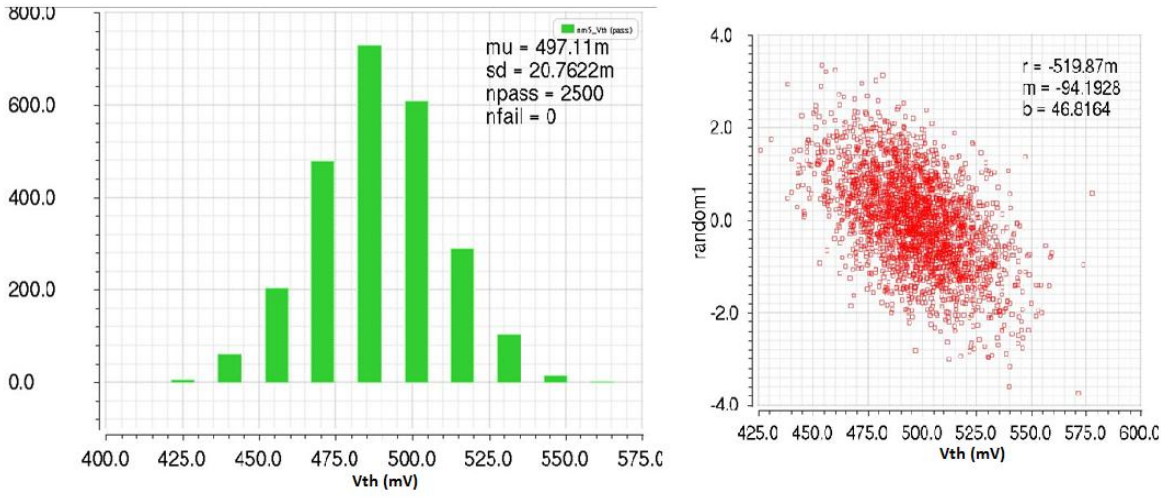

Figure 4: MC Simulation for Threshold Voltage of Transistor with N=2500

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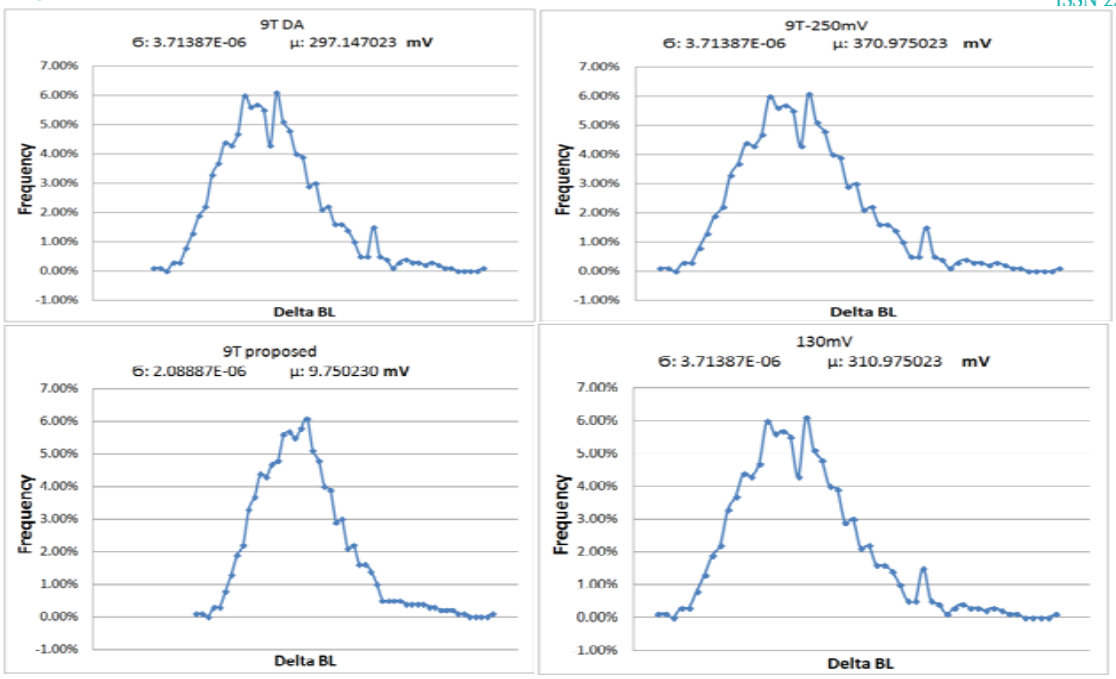

Figure 5: MC Simulation on Voltage Drop on ΔBL with N=1000

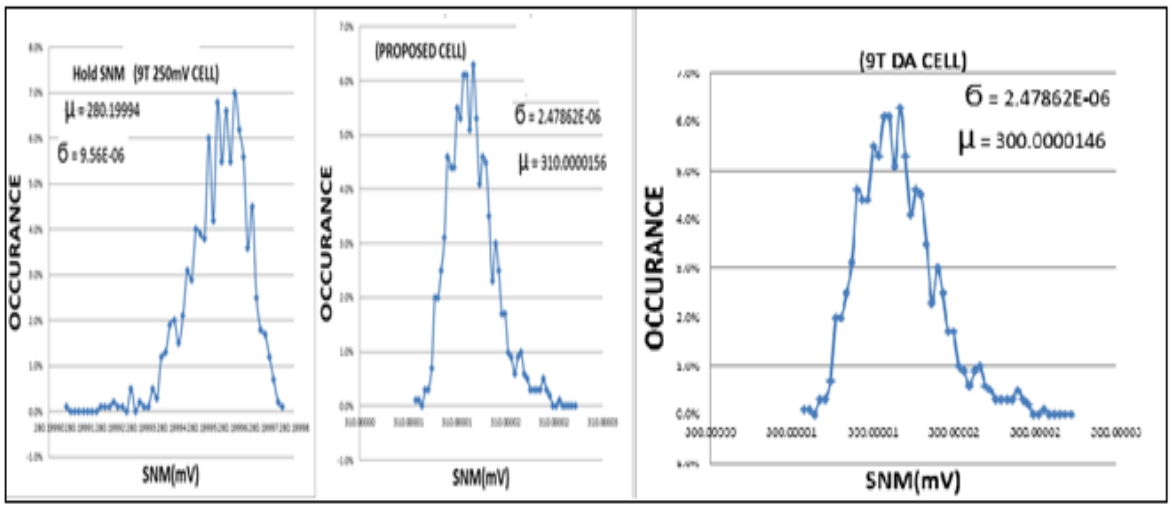

Figure6(a): MC Simulation for Hold Mode with N=1000

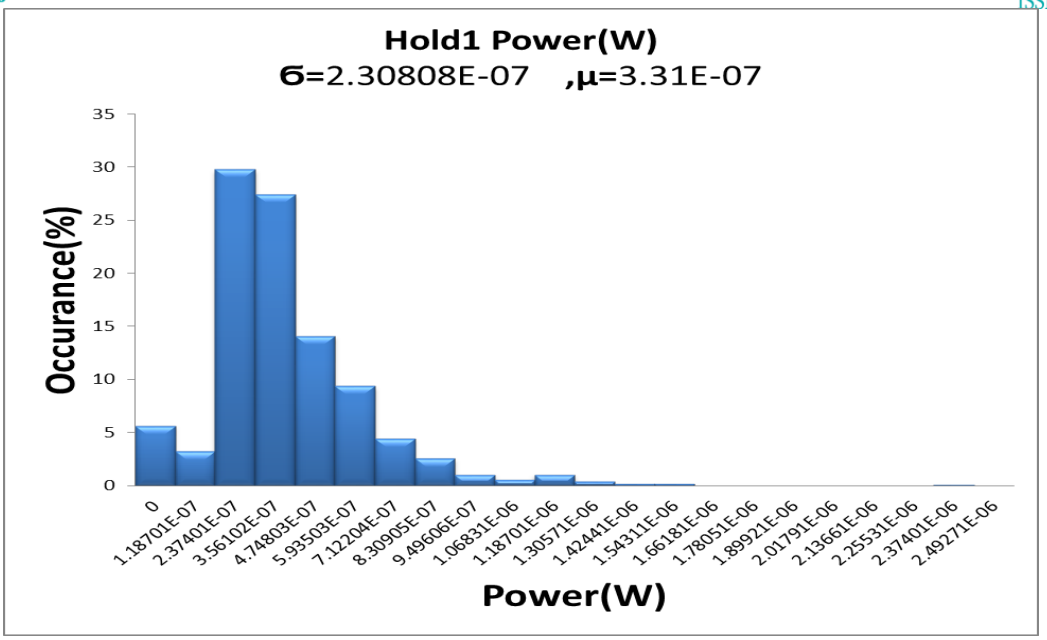

Figure6(b): MC Simulation for Hold Power with N=1000

The simulation to see the statistical variation on the storage nodes value with WS, we run the MC simulation for N=1000 as shown in Figure 7. It is seen from Figure that as long as WS is maintained at its desired value, the storage nodes Q and QL are clamped to their strong logic.

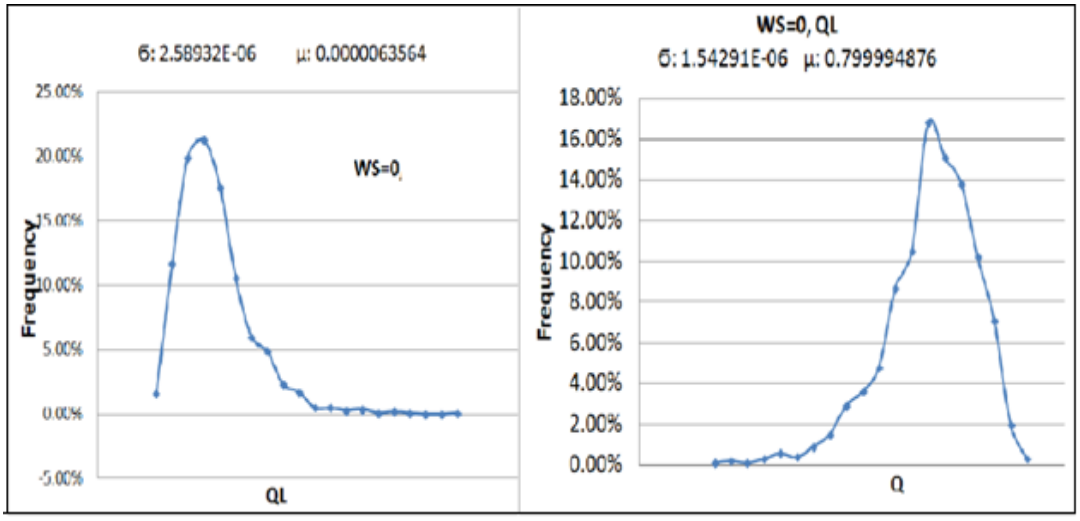

Figure 7: MC Simulation for Write Ability at Vdd=0.8V

IV. CONCLUSION

The proposed cell reduces the dynamic power as well as leakage power appreciably during write/read operation. The write ability of the cell is increased due to separate write signal WS. The proposed cell shows robustness against any global and local variations as well as temperature due to lower discharging activity, lower leakage current, separate write signal WS and separate port for read/write operation.

V. ACKNOWLEDGMENT

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