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HARDWARE BASED RECOVERY OF SAMPLE TIMING FOR UNDERRUN/OVERRUN CONDITION IN DOWNLINK (DL) AND UPLINK (UL) PATH OF BASE BAND RNC/ENODEB

Puneet Khandelwal[1], Somvir Dahiya[2], Arvind Kaushik[3]

[1,2]Senior Design Engineer Lead, [3]Senior Member of Technical Staff, Freescale Semiconductor, Noida (India)

ABSTRACT

*The Common Public Radio Interface (CPRI) is a key interface of radio base stations between the **R**adio **E**quipment **C**ontrol (REC) and **R**adio **E**quipments (RE). It connects multiple REC and RE in the network working at high data rates (up to 12.16512Gbps). CPRI is a high speed streaming protocol with no retransmission capabilities. CPRI Link works in a continuous operation in real time. There can be catastrophic scenarios, such as, link to antenna sub-system starves and causes underrun condition in DL path and overrun condition in UL path. This article explains relatively simple hardware implementation that can remove the software dependency in handling sample alignment in DL/UL path in case of underun or overrun.*

Keywords: CPRI, Underun, Overrun, Sample alignment.

I. INTRODUCTION

The Common Public Radio Interface (CPRI) is a key interface of radio base stations between the Radio Equipment Control (REC) and Radio Equipments (RE). It connects multiple REC and RE in the network working at high data rates (up to 12.16512 Gbps). CPRI is a high speed streaming protocol with no retransmission capabilities. CPRI Link works in a continuous operation in real time.

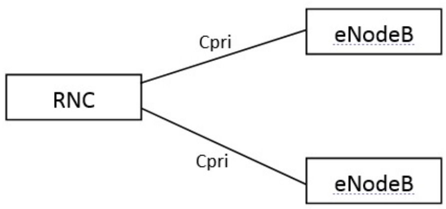

Figure 1. CPRI based E-UTRAN

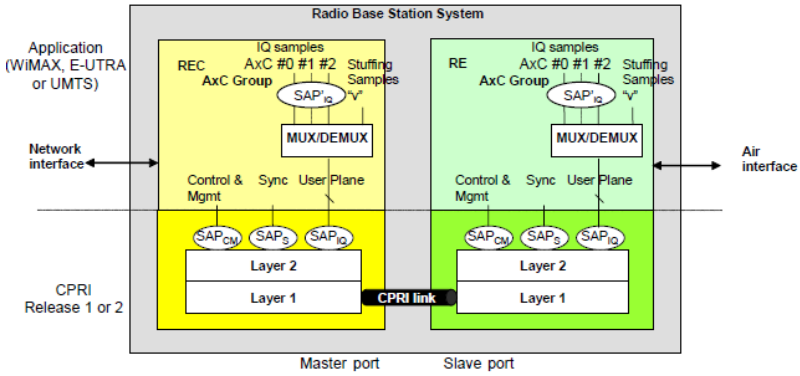

Figure 2. Example of Protocol Stack Based Upon CPRI

II. SYSTEM CASES FOR UNDERRUN AND OVERRUN

Baseband SoCs are getting complex due to scale of miniaturization and effort to reduce BOM cost of system. These SoCs have limited resource on interconnect BW, memories and processing resources. There can be catastrophic scenarios in which link to antenna sub-system starved and causes underrun condition in DL path and overrun condition in UL path. In this scenario the traffic from particular REC can get impacted.

III. ISSUES DUE TO UNDERRUN AND OVERRUN

While recovering from any underun or overrun condition in tradition manner, if software fails in successful recovery and data alignment process, system has to go through reset, startup and auto negotiation sequences. A sequence of actions needs to be performed by master and slave ports connected by CPRI in startup as shown in figure 3.

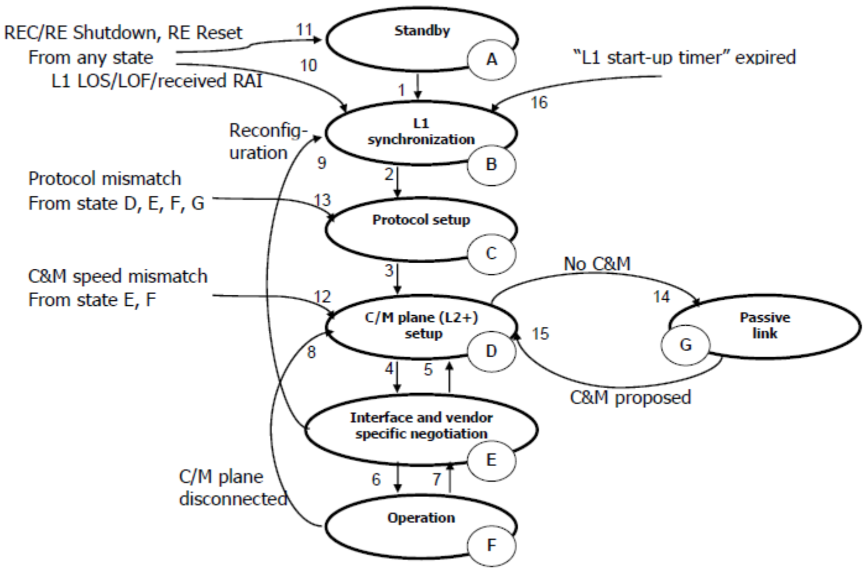

Figure 3. Start-up States and Transitions Defined by CPRI

Auto negotiation stage includes different steps mentioned below:

- Selecting Link rate between the devices.
- Selecting common C&M channel rate.
- Auto-detection of REC data flow on slave ports
- Selecting scrambling and scrambling seed.

To understand the impact of these steps, we can look into clock start-up time requirement defined by CPRI. CPRI shall enable the RE clock to achieve synchronization with respect to the frequency accuracy and absolute frame timing accuracy within 10 seconds.

Assuming maximum clock synchronization time (i.e. 10sec) and CPRI is operating at line rate option 9 (12. 16512 Gbps), penalty from re-synchronization itself is 15.2GByte.

The impact is even higher due to conditions as listed below:

- The QOS and connectivity of all users under affected REC will get impacted due to delay in restart operation.
- There is MIPS load on software to do restart operation and then synchronize the operation
- There is MIPS load on software to bring the context back on the link
- Abrupt reset can cause spectrum violation.
- Signal indeterminism can create signal peaks which can damage the eNodeB Power Amplifier (PA).
- Sudden power peaks can damage the User Equipment (UE).

IV. SOFTWARE SOLUTION

To recover from underrun or overrun scenario, software needs to shutdown CPRI subsystem along with Hardware accelerators if any. Once CPRI subsystem is shut down, it will take 20ms in coming back to normal operation that it equivalent to 2 CPRI radio frames. Assuming that CPRI is operating at line rate option 9 (12. 16512 Gbps), penalty from sub system shut down itself is 30.4MByte.

Apart from this, software needs to inform other REC or RE connected through it that it is stopping transmission or receiving so that other end can ignore the receiving samples or stop providing samples. Thus software solution involves both sides of a CPRI connection.

Even after this, software needs to make sure the alignment of data, once again after recovery because once alignment of samples is lost, processed data will be incorrect.

If software could not handle this complete recovery process including data alignment successfully, system has to go through reset, startup and auto negotiation sequences described above. Software again needs to do extra calculation to achieve the re-synchronization on the link. It also needs to bring the context back on the link now. This impacts system badly and affects the QOS.

V. HARDWARE SOLUTION

A relatively simple hardware implementation can remove the software dependency in system timing recovery and handling sample alignment in DL and UL path in case of underun or overrun.

HW solution addresses all limitation and offloads the recovery operation at link from software.

5.1 Detail of Hardware Solution in Case of Underrun Scenario

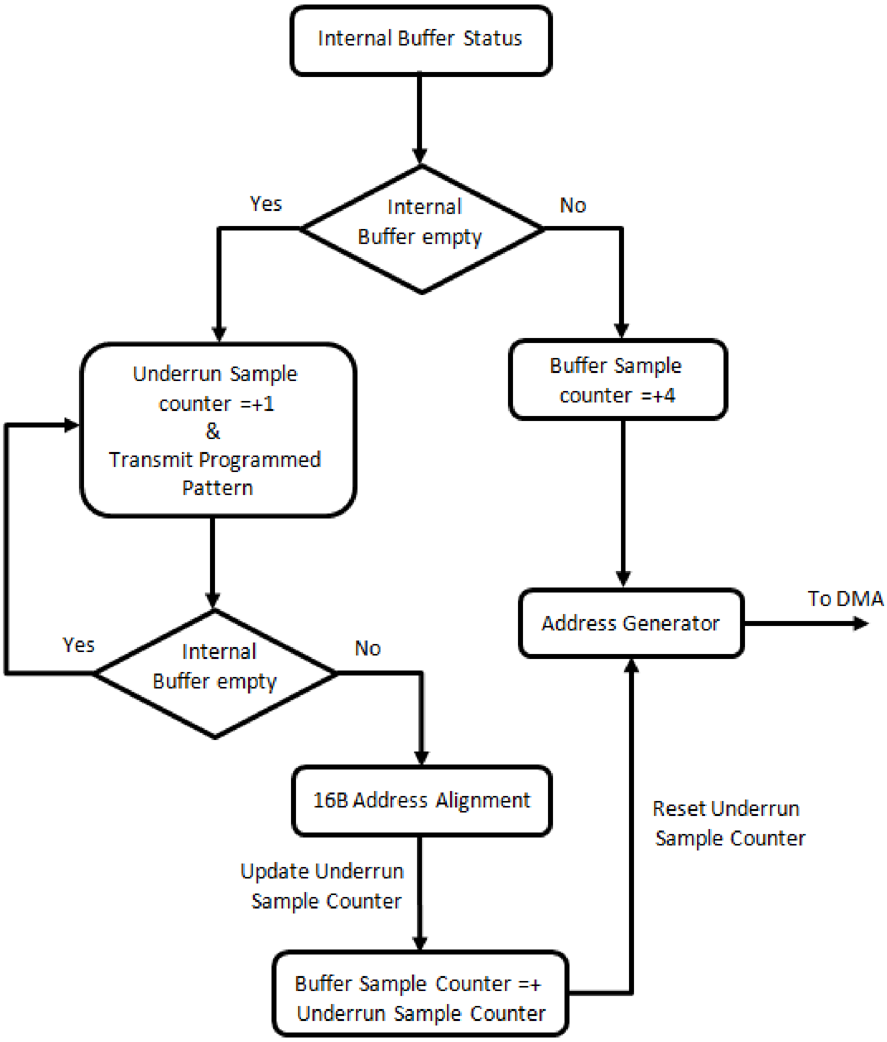

Figure 4. Underrun Recovery Flow Chart

5.2 Example of Underrun Recovery

Let's take an example where CPRI sub-system is having internal buffers with 32 bit word size and data is read from system memories through AXI interface with data bus width of128 bit. CPRI sub-system is AXI master and reading data from system memory, keeping it in internal buffers before finally transmitting it on link.

Assuming that due to Bandwidth crunch at AXI, CPRI sub-system starved and internal buffers hit underrun as shown below. CPRI start transmitting pre-programmed pattern on the link.

As soon as, system comes out of underrun, recovery mechanism updates internal sample counter and generates modified address for next read cycle from system memories as shown below.

It should be noted that in underrun conditions, a fixed pattern is being transmitted. It helps in preventing accidental damage of PA due to continuous high value samples.

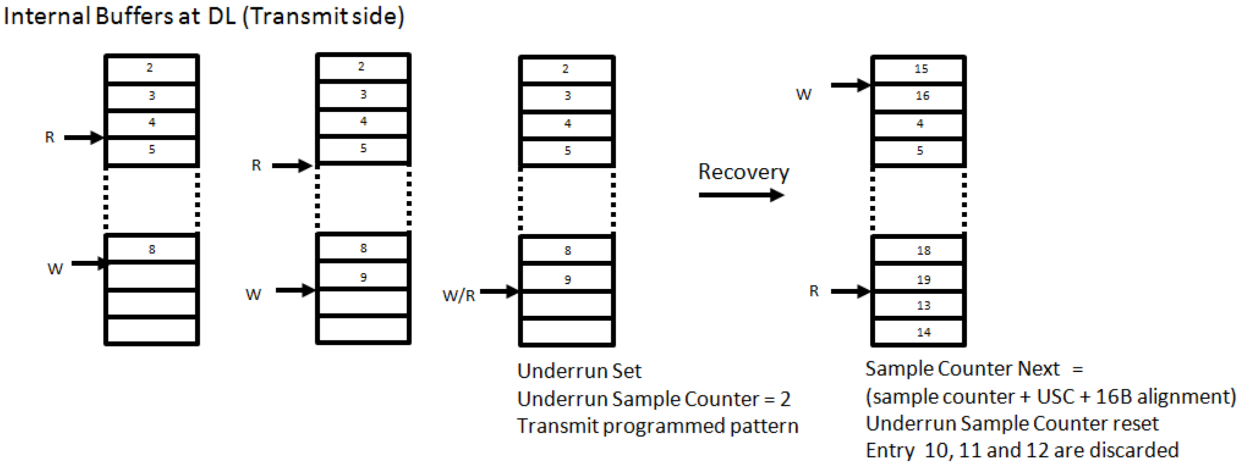

Figure 5. Underrun Recovery Example

5.3 Detail of Hardware Solution in Case of Overrun Scenario

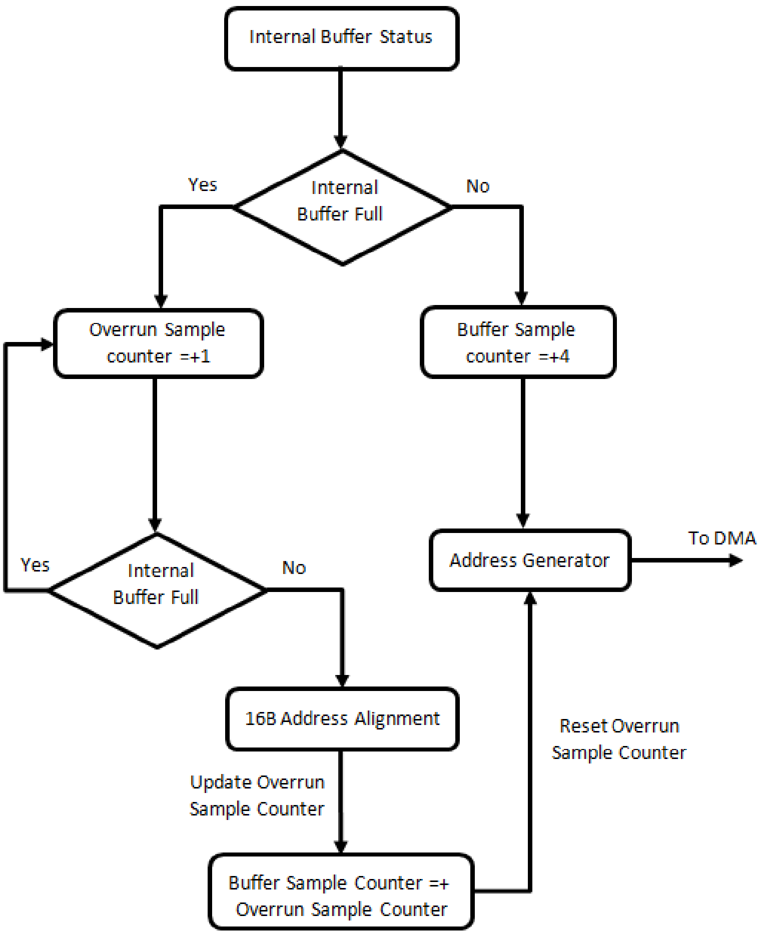

Figure 6. Overrun Recovery Flow Chart

5.4 Example of Overrun Recovery

Let's take an example where CPRI sub-system is having internal buffers with 32 bit word size and data is being written in system memories through AXI interface with data bus width of128 bit. CPRI sub-system is AXI master which is keeping data in internal buffers after receiving it from link before finally writing data in system memory.

Assuming that due to Bandwidth crunch at AXI, CPRI sub-system couldn't get write response from system side and internal buffers hit overrun as shown below.

As soon as, system comes out of overrun, recovery mechanism updates internal read pointer and generates modified address for next write cycle to system memories as shown below.

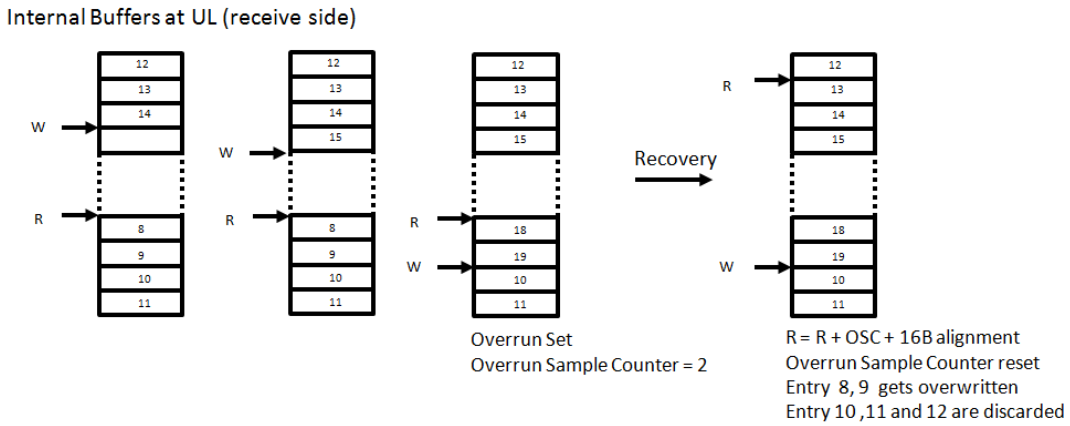

Figure 7. Overrun Recovery Example

VI. CONCLUSION

HW solution described in this paper offloads the recovery operation at link from SW efficiently and addresses all limitation mentioned below.

- It improves the recovery delay greatly.
- It offloads software MIPS for both underun and overrun scenarios.
- It handles data alignment efficiently after recovery.
- It prevents accidental damage to PA or sudden power peaks.
- It improves QOS of overall system.

Though there still might be some catastrophic conditions at RE or REC like complete system hung which cannot be recovered without system reset but proposed HW solution efficiently separate those situations from solvable situations like intermittent delays at interconnect etc.

After comparing both solutions, it becomes apparent that HW solution has great merits over SW solution. It works as a firewall for complete system in case of catastrophic conditions of underrun and overrun. It also helps in brining system back to normal conditions with minimum hit possible. It can be safely deduce that HW solution, to handle underrun and overrun scenarios, described in this paper is right choice for any CPRI sub-system.

REFERENCES

Protocol:

[1] CPRI Specification V6.1, http://www.cpri.info/spec.html